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FPGA HARDWARE DESIGN ENGINEER
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Key Accomplishments with FPGAs

- Accelerated a floating point matrix multiplication algorithm for large arrays
- Generated and monitored Ethernet packet streams for testing products against standards
- Decoded an array of MPEG video streams for IP core development
- Created a dynamic equalization architecture for QPSK signaling from optical networks
- Performed data acquisition and image reconstruction for medical PET scanners
- Implemented high-speed, self-calibrating ADC interface for signal processing
- Adapted Direct Digital Synthesis (DDS) for multiple applications in electronic warfare (EW)

Expertise

- 100-500+ MHz fabric clocking
- Xilinx UltraScale/Virtex/Zynq families
- VHDL and Verilog
- Designing for synthesis
- DDR3/HMC Memory Links
- Vivado IP Packaging and Scripting
- 10G/40G/100G+ bps bandwidths
- Computer architecture optimization
- Floorplanning
- Timing and Performance Analysis
- Project management and documentation
- Simulation for Functional Verification

EDA Tools and Software

- FPGA BACKEND: Xilinx Vivado/ISE, Altera Quartus II
- FPGA FLOORPLANNING & DEBUG: Xilinx Vivado, PlanAhead and ChipScope
- SIMULATION: Mentor QuestaSim/ModelSim, Aldec Active-HDL and Viewlogic VCS
- SYSTEM DESIGN: MathWorks MATLAB
- EMULATION: Mentor Veloce Quattro system
- SYNTHESIS: Xilinx XST, Synplicity Synplify, Mentor Precision, Synopsys Design Compiler
- SOFTWARE: C, Python, Fortran and Assembly
- SCRIPTS: Tcl, Python, Linux/Unix/DOS shell
- REVISION CONTROL: Subversion, CVS, Perforce
- DOCUMENTATION: MSWord, Visio

Published Work

- "*A Practical Measure of FPGA Floating Point Acceleration for High Performance Computing,*" IEEE International Conference on Application-specific Systems, Architectures, and Processors—ASAP2013, Washington, D.C., June 2013

Professional Highlights

Silvus Technologies (Broadband Wireless) **2016-2017**

Expert FPGA Developer

- While targeting the Xilinx UltraScale Kintex XCKU115, provided research, guidance, and an in-depth FPGA Performance Analysis Report on maximizing timing closure margins and optimal utilization of FPGA resources for a 100 Gbps RF Backbone System featuring the company's MIMO Equalization Algorithm
- Ran many build iterations (synthesis + implementation) while addressing and remedying persistent timing violations, typically modifying RTL code and constraints to achieve deterministic timing closure

NEC Laboratories America (Optical Transmission Systems) **2015-2016**

Expert FPGA Developer

- Targeting the Xilinx Zynq XC7Z030 for a Distributed Acoustic Sensing application, designed and simulated a four-channel 250 MSPS ADC front end receiver with a 10GE backend and hardware-initiated DMA capability
- The ADC interface supported the QDR-mode timing of the TI ADS42LB69 ADC and included auto-calibration of clock and bit recovery using Xilinx 7 Series IDELAY and ISERDES
- The 10GE portion, which was created as user IP and instantiated twice to create a 2x10GE port, was customized to include RXAUI on the back end while applying a special conversion at the front end to encapsulate raw and DSP-processed data into Ethernet frames

Giga-tronics (Electronic Warfare) **2015-2017**

Expert FPGA Developer

- Targeting the Xilinx Virtex-6 XC6VSX315T for this RF/DSP application, re-designed an entire architecture responsible for controlling and interacting with an assortment of RF components such as DACs, ADCs, VCO, PLL, Switches, and Filters for Arbitrary Waveform Generator (AWG) and up-converter Advanced Signal Generator (ASG) applications
- The two main reasons for the re-design was (a) to make timing closure deterministic, and (b) to extract the clogging host-access logic from the line-rate data and control paths
- Architecture featured a bank of Direct Digital Synthesis (DDS) IP cores for generating a sinusoidal waveform sample stream to an external DAC
- An embedded soft-core MicroBlaze processor was used for low-level access of the FPGA register and RAM space

CACI @ Aberdeen Proving Ground, MD (Electronic Warfare) **2015-2017**

Firmware Designer, Lead

- Managed team of firmware developers in sustaining and enhancing jamming equipment used to combat Radio Frequency (RF) threats. Leadership role included creating an entire firmware development infrastructure based on available resources, operating procedures, and task management.
- Created several architectures for Direct Digital Synthesis (DDS) applications, including waveform synthesis, frequency/phase/amplitude modulations, frequency sweeps, and quadrature signaling. Trained personnel on nuances of DDS sinusoidal generation.
- Designed a Multirate Resampler based on systolic operation of chained Xilinx DSP48 MACs (Multiply-Accumulate) and an optimized control scheme for handling the interpolation and decimation simultaneously.

Professional Highlights (continued)

Xilinx Inc. (Network IP Development and Verification) **2013-2015**

FPGA IP Architect

- Designed a Hybrid Memory Cube (HMC) transport layer adapter link between an HMC controller core and an HMC memory model for emulation purposes.
- Created packaging scripts for an entire portfolio of packet processing SDNet IP to standardize customer delivery and to ease the IP integration process within the Xilinx Vivado IP Integrator (IPI) infrastructure. Script flow included IEEE P1735 and AES128 encryption options.
- Researched, proposed, and led the implementation of a UVM verification environment for Ethernet switch and Traffic Manager (TM) IP.
- Led the adoption of the Mentor Veloce emulator system for the verification of the TM IP. This resulted in a sim speedup of 500x, reducing weeks of regression testing to one overnight run.

Optimal Design Inc. (High Performance Computing) **2012-2013**

FPGA Design Engineer

Implemented a double precision floating point matrix multiplication algorithm for HPC scientific applications. While targeting the Xilinx Virtex-7 VX690T, used advanced floorplanning techniques to reach timing closure at 500 MHz for an overall sustained performance of 144 GFLOPS, with proposed improvements to reach 180 GFLOPS. Maximized sustained throughput by using systolic MAC array processing, an optimized data caching/re-use scheme, and a balanced I/O streaming mechanism while running two DDR3 memory links at maximum efficiency. Presented research at IEEE ASAP 2013 (see "Published Work" above).

Sencore Inc. (Broadcast Video Delivery Products) **2011**

FPGA Design Engineer

Designed an MPEG Video Transport Stream FPGA targeting the Xilinx Spartan-6 XC6SLX45T for company's next generation video decoder product. Architecture included serial 270 Mbps ASI video ports, 2.7 Gbps SERDES video ports, and a direct parallel transport link to the Magnum D7Pro digital media processor chip. FPGA also performed BISS-E stream decryption while applying descrambling keys dynamically extracted from incoming PIDs.

NEC Laboratories America (DSP for 100G Optical Networks) **2009-2011**

FPGA Design Engineer

- Evaluated mega-array of *Xilinx FFT* cores for performance and device packing utilization within select Virtex-5 and Virtex-6 devices.
- Designed a *1.5x-to-2x Resampler* module comprised of FIR filtering, interpolation, and down-sampling functions optimized into a single-clocked convolution of coefficients and input samples.
- Designed a quad-channel *Dynamic Equalizer FPGA for QPSK signaling* within a Virtex-5 SX240T device. Architecture included an array of FFTs so that DSP-intensive arithmetic processing could be executed in the frequency domain. Reached timing closure with 60% of design clocked at 357 MHz and with 80% utilization of available DSP48 and BRAM cores.

Professional Highlights (continued)

Circadiant Systems, Inc. (Optical Standards Test Equipment) **2001-2009**

Chief FPGA Design Engineer

Responsible for developing the digital infrastructure for the company's OST products. Primary responsibilities included the following designs:

- A *10GE/SONET/PoS Pattern Generation & BERT Analysis* Xilinx XC2V6000 FPGA used for transmitting PRBS patterns, packets, and user-defined data while performing BERT analysis and protocol monitoring of received traffic. Architecture included PCI target core.
- A *Crosspoint Switch* Xilinx XC2V6000 FPGA which enabled full-duplex communication between Pattern Generation and BERT Analysis FPGA (above) and AMCC's *Khatanga* SONET framer and *Hudson* Digital Wrapper/FEC devices. Architecture supported 622/644/669 MHz operation to meet SONET (9.95Gbps), 10GbE LAN (10.304Gbps), and OTN (10.709Gbps) requirements, featuring FPGA fabric running at a top rate of 335 MHz.
- *A 10G Ethernet Protocol core* comprised of a frame generator and protocol checking logic used in conjunction with 10GE MAC and Physical Coding Sub-layer (PCS) cores.

Nearfield Systems, Inc. (Antenna Measurement) **2007-2008**

FPGA Design Engineer

Enhanced the antenna measurement capabilities of a PowerPC-based digital processing board targeting a Virtex-4 LX100 FPGA by creating an eight-port DDR2 Memory Arbitration module with BIST capability, and a proprietary high-speed SERDES link based on a quadrature clock-data recovery scheme.

Xilinx Corp. (Video Decoder Core) **2005-2006**

FPGA Design Engineer

Developed an MPEG-4 decoder core for multiple video streams, which involved extracting Video Object Plane (VOP) and Macroblock data information encrypted with variable-length codes (VLC's). Targeted Xilinx Virtex-4 and Spartan-3 families.

Sarnoff Real Time Corp./DIVA Corp. (Video-on-Demand) **1996-1999**

FPGA Design Engineer

Developed Altera 10K200E FPGA-based designs for various MPEG packet processing functions within the company's Video-on-Demand (VOD) servers, including a Crosspoint Switch, a Rate Controller, and a Packet Transfer Controller.

UGM Medical Systems (Medical Imaging) **1991-1995**

Head of Hardware Engineering

Designed several VME-based 9Ux400mm PCBs for company's PET scanner using an assortment of Xilinx 4000-series FPGA designs for handling the bulk of the digital processing. These PCBs included:

- a 48-channel data acquisition PCB for digitizing and recording radioactive photon-pair "events" for coincidence imaging / a position processing unit based on a "local centroid position" algorithm for calculating the energy and position of each radioactive event / a Sinogram Reconstruction and Distortion Removal PCB for volume image pre-processing prior to upload into a host workstation for final image reconstruction.

Education

- MSEE, Drexel University, Electrical and Computer. Engineering Emphasis on digital design, computer architecture, and systolic arrays (GPA: 3.9/4.0).
- BSEE, Drexel University, Electrical and Computer Engineering.