

Expertise

- 10-600+ MHz Digital Designs
- Xilinx Virtex-5, -6, -7 Families
- Timing and Performance Analysis
- System Test and Debug
- High Performance Computing (HPC)
- VHDL and Verilog
- Computer architecture optimization
- Functional Simulation
- FPGA Floorplanning and Constraints
- Project Management and Documentation

EDA Tools and Software

- FPGA BACKEND: Xilinx ISE Design Suite, Altera Quartus II
- SIMULATION: Mentor ModelSim, QuickHDL, Viewlogic VCS
- SYNTHESIS: Xilinx XST, Synplcity Synplify, Mentor Precision and Leonard Spectrum
- FPGA FLOORPLANNING: Xilinx PlanAhead
- FPGA CHIP DEBUG: Xilinx Chipscope
- SCRIPTS: Embedded Linux, Xilinx build, ModelSim batch
- REVISION CONTROL: Subversion, CVS
- DOCUMENTATION: MSWord, Visio, EMA TimingDesigner
- SOFTWARE: C, Tcl, Fortran, Assembly

Current Research

2011-2012 HPC in FPGAs

Working to demonstrate the actual routed performance of the DGEMM ("Double Precision General Matrix Multiply") algorithm targeting the Xilinx Virtex-6 and Virtex-7 families. DGEMM is a fundamental benchmark for evaluating the performance of HPC machines. Keys to maximizing sustained throughput include systolic MAC array processing, an optimized data caching/re-use scheme, and an efficient means of balancing I/O streaming with the parallel processing of the MAC array. Key interfaces include a PCIe Gen3x8 port and two 64-bit DDR3 memory links.

Professional Highlights

2011 Sencore Inc. (Broadcast Video Delivery Products)

Design, simulation, and in-system test of an MPEG Video Transport Stream FPGA targeting the Spartan-6 XC6SLX45T for company's next generation video decoder product. In routing transport streams to and from video ports, architecture included serial 270 Mbps ASI video ports, 2.7 Gbps SERDES video ports, and a direct parallel transport link to the Magnum D7Pro digital media processor chip. FPGA was also responsible for performing stream decryption according to the BISS-E standard, with the added capability of applying descrambling keys dynamically according to incoming PIDs.

2009-2011 NEC Laboratories America (DSP for 100G Optical Networks)

Responsible for three separate but related projects:

- Evaluated mega-array of *Xilinx FFT* cores for performance and device utilization (i.e. packing) within select Virtex-5 and Virtex-6 devices.

- Designed a *1.5x-to-2x Resampler* module comprised of FIR filtering, interpolation, and down-sampling functions that were optimized into a single-clocked convolution of coefficients and input samples.
- Designed a quad-channel *Dynamic Equalizer FPGA for QPSK signaling* within a Virtex-5 SX240T device. Architecture included an array of FFTs so that DSP-intensive arithmetic processing could be executed in the frequency domain. Reached timing closure with over 60% of design clocked at 357 MHz while achieving 80% utilization of available DSP48 slices and BRAMs.

2001-2009 Circadiant Systems, Inc. (Optical Standards Test Equipment)

Chief FPGA architect responsible for developing the digital infrastructure for the company's OST products. Primary responsibilities included the following designs:

- A *10GE/SONET/PoS Pattern Generation & BERT Analysis* Xilinx XC2V6000 FPGA used for transmitting PRBS patterns, packets, and user-defined data while performing BERT analysis and protocol monitoring of received traffic.
- A *Crosspoint Switch* Xilinx XC2V6000 FPGA which enabled full-duplex communication between Pattern Generation and BERT Analysis FPGA (above), and AMCC's *Khatanga* SONET framer and *Hudson* Digital Wrapper/FEC devices. Architecture supported 622/644/669 MHz operation to meet SONET (9.95Gbps), 10GbE LAN (10.304Gbps), and OTN (10.709Gbps) throughput requirements.
- A *10G Ethernet Protocol core* comprised of a frame generator and protocol checking logic used in conjunction with 10GE MAC and Physical Coding Sub-layer (PCS) cores.
- *Embedded Control FPGA* for OST Chassis Blade that extended the GPIO and SPI/I2C facilities of an embedded Kontron X-Board 861 processor module for a PICMG 2.16 (CompactPCI) backplane. Main role of FPGA was direct control of optical components such as lasers and attenuators.

2007-2008 Nearfield Systems, Inc. (Antenna Measurement)

Enhanced the antenna measurement capabilities of a PowerPC-based digital processing board by adding the following functions to a Virtex-4 LX100 FPGA: (a) a proprietary high-speed SERDES link based on a quadrature clock-data recovery scheme, and (b) an eight-port DDR2 Memory Arbitration module, including built-in self test (BIST) capability.

2005-2006 Xilinx Corp. (Video Decoder Core)

Developed an MPEG-4 Variable-length decoder that supported multiple video streams, which involved extracting Video Object Plane (VOP) and Macroblock data information encrypted with variable-length codes (VLC's). Targeted Xilinx Virtex-4 and Spartan-3 families. Verification included functional simulation along with real-time testing on Xilinx' *Wildcard* platform PC Card.

1997-1999 Sarnoff Real Time Corp./DIVA Corp. (Video-on-Demand)

Developed Altera 10K200E FPGA-based designs for various MPEG packet processing functions within the company's Video-on-Demand (VOD) servers, including a Crosspoint Switch, a Rate Controller, and a Packet Transfer Controller FPGA.

1995-1996 Lucent Technologies (LAN/Telecom)

Designed a PCMCIA Card for interfacing an ATM LAN adapter module to a mobile computer within the range of a broadband services network. The PC Card bus controller incorporated wireless internet access capability using two IDT 72V255 SuperSYNC FIFOs as transmit and receive buffers.

1991-1994 UGM Medical Systems (Medical Imaging)

Designed several VME-based 9Ux400mm PCBs for company's PET Scanner using an assortment of Xilinx 4000-series FPGA designs to do the bulk of the digital processing. These PCBs included: (a) a 48-channel data acquisition PCB for digitizing and recording radioactive photon-pair "events" for coincidence imaging, (b) a position processing unit based on a "local centroid position" algorithm for calculating the energy and position of each radioactive event, and (c) a Sinogram Reconstruction and Distortion Removal PCB for volume image pre-processing prior to upload into a host workstation for final image reconstruction.

Recommendations

“John's FPGA expertise was invaluable to our team at NEC Labs America in our investigation of DSP equalization techniques for 100G optical networks.”

Junqiang Hu, Research Staff Member, NEC Labs America (jqhu@nec-labs.com)

“John is one of the best design engineers I have ever worked with.”

Steve Zack, Design Engineer, DIVA and Xilinx (stevenzack@comcast.net)

“In addition to John's technical excellence, he is great to work with because of his good natured personality, responsiveness and overall professionalism.”

Craig Javid, Hardware Consultant, Nearfield Systems (craig.javid@roadrunner.com)

“John's organizational ability allowed the group to deliver very innovative solutions on the committed date and the FPGAs worked.”

John French, Co-founder, Circadiant Systems Inc. (John.si.French@gmail.com)

“John was the sole contributor / developer for many of the company's FPGA designs. He possesses a deep technical understanding of complex systems and system interactions. He was a great person to work with and a great resource to the company.”

Sheldon Sun, Hardware Engineer, Circadiant Systems Inc. (ssun_98@yahoo.com)

Client List

- Circadiant Systems Inc.
- Cyberpath, Inc.
- DIVA (formerly Sarnoff Real Time Corp.)
- Federal Aviation Administration
- General Instrument Corp.
- IBM Corp.
- Inrange Technologies Corp.
- JDS Uniphase Corp.
- Judson Technologies
- Lucent Technologies, Inc.
- Motorola, Inc.
- NEC Laboratories America
- Nearfield Systems, Inc.
- Netquest Corp.
- Sarnoff Corp.
- Sencore Inc.
- Smiths Industries Aerospace
- SpectraSonics Imaging
- UGM Medical Systems, Inc.
- Xilinx Corp.

Membership

- Institute of Electrical and Electronic Engineers (IEEE)
- IEEE Computer Society
- Associate Member, Xilinx Alliance Program
- Society for American Baseball Research (SABR)